APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,216	11/26/2003	Nick Hilliard		1215

33148	7590	03/16/2005	

JUSTIN GRAY
12003 WALNUT BRANCH RD.
RESTON, VA 20194

EXAMINER
PAIK, STEVE S

ART UNIT	PAPER NUMBER
2876	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/707,216	Applicant(s) HILLIARD, NICK
	Examiner Steven S. Paik	Art Unit 2876

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _26 November 2003_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-7_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-7_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _herewith_.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Objections

1.   Claims 1-7 objected to because of the following informalities: claims 1-7 are numbered

as [c1]-[c7]. It is respectfully requested to replace them by 1, 2,...., and 7 in a consecutive and

sequential manner. Appropriate correction is required.

Re claim 5, please replace the word, "it" with -- the method -- if that's what the applicant

intends to claim.

Re claim 6, please replace the word, "it" with -- the method -- if that's what the applicant

intends to claim.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

3.   Claims 1-5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bauer et

al. (US 2003/0216969 A1) in view of Omelchenko (SU 656052A).

Re claims 1 and 7, Bauer et al. disclose a method and an apparatus to convert a UPC

format to an EPC format (page 16, [0176]-[0181]). The reference discloses the differences

between UPCs (may consist of decimal data) and EPCs (binary data) and how the conversion

process is performed.

However, Bauer et al. are silent about the claimed means of loading and storing registers

and the means of multiplying, dividing, shifting or adding register contents.

Omelchenko discloses a method and an apparatus for converting a binary-decimal number into a binary code. The conversion is attained by using logic gates, inhibit, adder, counter, shift register and binary equivalents memory. The circuit comprises, among other things, OR gates, and AND gates. The converter provides an increased operational speed by achieving simultaneous additions of lower and higher digits.

In view of Omelchenko, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to further employ an increased operational speed of BCD into binary-code conversion in addition to the conversion method of a UPC format to an EPC format of Bauer et al. due to the fact that faster conversion can be accomplished by simultaneously adding of lower and higher digits.

Re claim 2, Bauer et al. in view of Omelchenko discloses the method as recited in rejected claim 1 stated above, wherein the operation of storage of a register involves only shift operations (Binary adders contents are transferred sequentially through shift registers until equivalent binary code is established).

Re claim 3, Bauer et al. in view of Omelchenko discloses the method as recited in rejected claim 1 stated above, wherein the operation of storage of a register involves only multiplication or division operations (The De Morgan laws can be applied to optimize the number of logic gates and operations to produce any desired Boolean operation).

Re claim 4, Bauer et al. in view of Omelchenko discloses the method as recited in rejected claim 1 stated above, storage of a register involves a mix of multiplication, division, or shift operations (The De Morgan laws can be applied to optimize the number of logic gates and operations to produce any desired Boolean operation).

Re claim 5, Bauer et al. in view of Omelchenko discloses the method as recited in rejected claim 1 stated above, wherein the entire operation of the method or parts of it are embodied within digital logic gates (OR gates and AND gates).

4.   Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bauer et al. (US 2003/0216969 A1) as modified by Omelchenko (SU 656052A) as applied to claim 1 above, and further in view of Avgul et al. (SU 1429127A).

The teachings of Bauer et al. in view of Omelchenko have been discussed above.

Neither Bauer et al. reference nor Omelchenko discloses the operations are embodied within a Hamiltonian or other matrix operation.

Avgul discloses a matrix operations calculator comprising a plurality of registers, summator, multiplier, flip-flops, AND gates and NOT gates. The circuit realizes matrix operations to generate a desired output.

Therefore, it would have been obvious at the time the invention was made to a person having of ordinary skill in the art to have incorporated the matrix operations calculator as taught by Avgul into the teachings of Bauer et al. in view of Omelchenko for the purpose of maximizing the productivity within the step of operations involved with various logic gates.

Conclusion

5.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rothschild (US 6,651,053) discloses a conversion process of a UPC input into a different database.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven S. Paik whose telephone number is 571-272-2404. The examiner can normally be reached on Mon - Fri (5:30am-2:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on 571-272-2398. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven S. Paik
Primary Examiner
Art Unit 2876

ssp